Planning Test Strategies at Board level

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The test of complex VLSI systems is an activity where aspects of quality, time, cost, availability of equipment and design choices are important. Traditionally, the choice of testing at board level was simply a question of selecting one or more test stages to be used (for example in circuit test followed by functional test as part of a system). However, if a certain quality level has to be met, and, as is often the case in complex boards, accessibility is hampered by the use of methods such as surface mounting, or if a choice of ATE is available, or if different options are available for the components, it becomes clear that the traditional view is no longer adequate. It is important to redefine the term 'test strategy' as "the selection of design choices and test stages which will achieve the highest quality product at the lowest cost".

It becomes clear, therefore, that the test strategy options have to be examined before the completion of the board development, in order to accommodate possible changes in the board design. This highlight the need for predictive tools to calculate the cost and achievable quality of board test strategies. This work addresses a key area in chip design - test issues typically take up as much time as the functional design, but are often overlooked or underestimated. In addition, given the complexity of the problem, it is very difficult to ensure a high quality and cost effective test.

The authors have successfully used economics modelling techniques for ASIC test strategy planning, which have been incorporated in a test advisor system. This submission will provide examples of the use of economics models in the planning of board strategies. The models are fully parameterised and are part of an industrial testability advisor tool, which was developed as part of the ESPRIT EVEREST programme in association with Siemens-Nixdorf in Munich.

Cost models currently implemented

- **repair**
  Lists repair costs per defect type

- **iterations**
  Lists iteration factors for system design, layout, prototype production and verification

- **labrates**
  Labour rates for circuit design, circuit layout, prototype production and verification

- **board_data**
  Board information (number of components of each type, layers, nodes, sides, wire separation etc.)

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design_data: parameters describing design effort (in hours)
prod_data: production data and numbers of components of the same assembly type
assembly: assembly costs for specific assembly types
prod_cost: calculated production costs
def_spectrum: defect spectrum
component2fault: for each component, the number of actual faults arising from the defects present
test_stage: cost model specific to the test stage and test equipment used.
tot_cost: calculates the total cost based on the costs of the various stages

The user can examine the cost models in detail during the test strategy planning process. Quality levels and detailed fault cover at each stage, as well as costs, are important in determining the suitability of a test strategy. Fault spectrums for specific device types are implemented, and the user can select from different design alternatives (providing for example, boundary scan or different quality levels).

Four strategies were evaluated for an example board, with a production run of 5000 units:
- Functional test followed by system test
- Boundary scan, functional test, system test
- Pre-screen (using a manufacture defects analyser), functional test, system test
- Pre-screen, boundary scan, functional test, system test

The results showed that the boundary scan test strategies have a higher yield. They also showed that boundary scan not only improves the yield compared to functional test alone, but achieves this at a lower cost, despite the increase in the cost of boundary scan components. This is due to the ease of diagnosis that boundary scan offers over functional test. The use of boundary scan means that a reduced number of faults need to be diagnosed by functional test, thus effectively reducing the test costs. The effect can be seen in figures 1 and 2, showing the fault spectrum for the first two strategies (cost are in ECU, European Currency Units).
FAULT SPECTRUM
(functional test followed by system test)

![Fault Spectrum Graph]

Figure 1. Fault spectrum for functional test/system test
FAULT SPECTRUM
(boundary scan followed by functional test followed by system test)

![Fault Spectrum Graph](image)

Figure 2. Fault spectrum for boundary scan/functional test/system test